

## CLAIMS

1. A semiconductor integrated circuit device comprising:

(a) a first memory array area which includes a plurality of first memory cells and first data lines which are formed on a first layer and connected with said first memory cells;

(b) a second memory array area which includes a plurality of second memory cells and second data lines which are formed on said first layer and connected with said second memory cells;

(c) a sense amplifier area which includes sense amplifiers;

(d) a first connecting area located between said first memory array area and said sense amplifier area; and

(e) a second connecting area located between said second memory array area and said sense amplifier area,

wherein said semiconductor integrated circuit device further includes:

(f) first lines which are formed on a second layer different from said first layer and connected with said first data lines in said first connecting area; and

(g) second lines which are formed on said second layer and connected with said second data lines in said second connecting area,

said sense amplifiers being connected between said first lines and said second lines and adapted to amplify voltage differences between said first lines and said second lines.

2. A semiconductor integrated circuit device according to claim 1, wherein said first memory array area, said first connecting area, said sense amplifier area, said second connecting area, and said second memory array area are located to align in this order in the extending direction of said first and second data lines.

3. A semiconductor integrated circuit device according to claim 1, wherein said first memory array area, said first connecting area, said sense amplifier area, said second connecting area, and said second memory array area are areas having virtually rectangular shapes,

wherein said semiconductor integrated circuit device further includes a switch forming area which is located between said first memory array area and said first connecting area,

wherein said switch forming area includes data transfer lines (IO) and switch circuits having signal transfer paths which are connected between said first data lines and said data transfer lines, said data transfer lines being formed on said second layer to extend in a direction which intersects said first lines.

4. A semiconductor integrated circuit device according to claim 2, wherein said first and second lines are laid out over said sense amplifier area.

5. A semiconductor integrated circuit device according to claim 2, wherein at least part of said first and second lines

are laid out over said sense amplifier area.

6. A semiconductor integrated circuit device according to claim 2, wherein said second layer is an upper layer relative to said first layer.

7. A semiconductor integrated circuit device according to claim 2, wherein said first and second lines are formed to extend in the extending direction of said first and second data lines.

8. A semiconductor integrated circuit device according to claim 1 further including word lines which intersect said first and second data lines at right angles, said memory cells being formed at all intersections of said first and second data lines and said word lines and each made up of a data transfer MISFET and a capacitor, with the gate electrode of said MISFET being connected to a word line.

9. A semiconductor integrated circuit device according to claim 1, wherein said first lines, second lines, first data lines and second data lines are formed by use of a Levenson's line-and-space mask which is coated with shifters of alternately different phases.

10. A semiconductor integrated circuit device according to claim 1, wherein said first and second data lines have a virtually equal line spacing.

11. A semiconductor integrated circuit device according to claim 1, wherein said first and second lines and said first

and second data lines have a line spacing which is equal to a minimum working dimension.

12. A semiconductor integrated circuit device according to claim 1, wherein said memory cells are each formed in an area having a size of  $4F^2$  (where F denotes a minimum working dimension).

13. A semiconductor integrated circuit device comprising:

(a) first data lines which are formed to extend in a first direction on a first layer and connected with a plurality of first memory cells;

(b) second data lines which are formed to extend in the first direction on said first layer and connected with a plurality of second memory cells;

(c) first lines which are formed to extend straight in the first direction on a second layer different from said first layer and connected with said first data lines;

(d) second lines which are formed to extend straight in the first direction on said second layer and connected with said second data lines; and

(e) sense amplifiers which are connected to said first lines and said second lines and adapted to amplify voltage differences between said first lines and said second lines.

14. A semiconductor integrated circuit device according to claim 13 further including word lines which intersect said first and second data lines at right angles, said memory cells

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being formed at all intersections of said first and second data lines and said word lines and each made up of a data transfer MISFET and a capacitor, with the gate electrode of said MISFET being connected to a word line.

15. A semiconductor integrated circuit device according to claim 13, wherein said first lines, second lines, first data lines and second data lines are formed by use of a Levenson's line-and-space mask which is coated with shifters of alternately different phases.

16. A semiconductor integrated circuit device according to claim 13, wherein said first and second data lines have a virtually equal line spacing.

17. A semiconductor integrated circuit device according to claim 13, wherein said first and second lines and said first and second data lines have a line spacing which is equal to a minimum working dimension.

18. A semiconductor integrated circuit device according to claim 13, wherein said memory cells are each formed in an area having a size of  $4F^2$  (where F denotes a minimum working dimension).

19. A semiconductor integrated circuit device comprising:

(a) first data lines which are formed to extend in a first direction on a first layer and connected with a plurality of first memory cells;

(b) second data lines which are formed to extend in the

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first direction on said first layer and connected with a plurality of second memory cells;

(c) first lines which are formed to extend straight only in the first direction on a second layer different from said first layer and connected with said first data lines;

(d) second lines which are formed to extend straight only in the first direction on said second layer and connected with said second data lines; and

(e) sense amplifiers which are connected to said first lines and said second lines and adapted to amplify voltage differences between said first lines and said second lines, said first and second lines being laid out over said sense amplifiers.

20. A semiconductor integrated circuit device comprising:

(a) first data lines which are formed to extend in a first direction on a first layer and connected with a plurality of first memory cells;

(b) second data lines which are formed to extend in the first direction on said first layer and connected with a plurality of second memory cells;

(c) sense amplifiers which amplify voltage differences between said first data lines and said second data lines;

(d) first lines which are formed to extend in the first direction on a second layer which is an upper layer relative to said first layer, and are connected between said first data

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lines and said sense amplifiers;

(e) second lines which are formed to extend in the first direction on said second layer and connected between said first data lines and said sense amplifiers; and

(f) precharge lines (VBLR) adapted to feed a precharge voltage to said first and second data lines,

wherein said precharge lines are formed to extend in a second direction perpendicular to the first direction on said first layer.

21. A semiconductor integrated circuit device comprising:

(a) first data lines which are formed to extend in a first direction on a first layer and connected with a plurality of first memory cells;

(b) second data lines which are formed to extend in the first direction on said first layer and connected with a plurality of second memory cells;

(c) sense amplifiers which amplify voltage differences between said first data lines and said second data lines;

(d) first lines which are formed to extend in the first direction on a second layer which is an upper layer relative to said first layer, and are connected between said first data lines and said sense amplifiers;

(e) second lines which are formed to extend in the first direction on said second layer and connected between said second data lines and said sense amplifiers; and

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(f) power lines (CSN) adapted to feed a power voltage to said sense amplifiers,

wherein said power lines are formed to extend in a second direction perpendicular to the first direction on said first layer.

22. A semiconductor integrated circuit device comprising:

(a) first data lines which are formed to extend in a first direction on a first layer and connected with a plurality of first memory cells;

(b) second data lines which are formed to extend in the first direction on said first layer and connected with a plurality of second memory cells;

(c) sense amplifiers which amplify voltage differences between said first data lines and said second data lines;

(d) first lines which are formed to extend in the first direction on a second layer which is an upper layer relative to said first layer, and are connected between said first data lines and said sense amplifiers;

(e) second lines which are formed to extend in the first direction on said second layer and connected between said second data lines and said sense amplifiers; and

(f) ground lines (CSP) which are formed to extend in a second direction perpendicular to the first direction on said first layer and adapted to feed a ground voltage to said sense amplifiers.

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23. A semiconductor integrated circuit device comprising:

(a) first data lines which are formed on a first layer and connected with first memory cells;

(b) second data lines which are formed on said first layer and connected with second memory cells;

(c) sense amplifiers which amplify voltage differences between said first data lines and said second data lines;

(d) first lines which are formed on a second layer which is an upper layer relative to said first layer, and are connected between said first data lines and said sense amplifiers;

(e) second lines which are formed on said second layer and connected between said second data lines and said sense amplifiers; and

(f) voltage lines (CSP, CSN) adapted to feed voltages to said sense amplifiers,

wherein said voltage lines are formed on said first layer to extend in a direction which intersects said first lines.

24. A semiconductor integrated circuit device comprising:

(a) a first memory array area which includes a plurality of first memory cells and first data lines which are formed on a first layer and connected with said first memory cells;

(b) a second memory array area which includes a plurality of second memory cells and second data lines which are formed on said first layer and connected with said second memory cells;

(c) a sense amplifier area which includes sense amplifiers;

(d) a first connecting area located between said first memory array area and said sense amplifier area;

(e) a second connecting area located between said second memory array area and said sense amplifier area; and

(f) a switch forming area which is located between said first memory array area and said first connecting area,

wherein said semiconductor integrated circuit device further includes:

(g) first lines which are formed on a second layer different from said first layer and connected in said first connecting area to said first data lines;

(h) second lines which are formed on said second layer and connected in said second connecting area to said second data lines,

said switch forming area including data transfer lines (IO) and switch circuits having signal transfer paths which are connected between said first data lines and said data transfer lines, and

said data transfer lines being formed on said first layer to extend in a direction which intersects said first lines.

25. A semiconductor integrated circuit device comprising:

(a) a first memory array area which includes a plurality of first memory cells and first data lines which are formed

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on a first layer and connected with said first memory cells;

(b) a second memory array area which includes a plurality of second memory cells and second data lines which are formed on said first layer and connected with said second memory cells;

(c) a sense amplifier area which includes sense amplifiers;

(d) a first connecting area located between said first memory array area and said sense amplifier area;

(e) a second connecting area located between said second memory array area and said sense amplifier area; and

(f) a switch forming area which includes switch circuits connected between said first data lines and data transfer lines,

wherein said semiconductor integrated circuit device further includes:

(g) first lines which are formed on a second layer different from said first layer and connected in said first connecting area to said first data lines; and

(h) second lines which are formed on said second layer and connected in said second connecting area to said second data lines,

said switch forming area being formed between said sense amplifier area and said first connecting area, with lines different from said first and second lines and formed on said second layer over said switch forming area.

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26. A semiconductor integrated circuit device comprising:

(a) a first memory array area which includes a plurality of first memory cells and first data lines which are formed on a first layer and connected with said first memory cells;

(b) a second memory array area which includes a plurality of second memory cells and second data lines which are formed on said first layer and connected with said second memory cells;

(c) a sense amplifier area which includes sense amplifiers;

(d) a first connecting area located between said first memory array area and said sense amplifier area;

(e) a second connecting area located between said second memory array area and said sense amplifier area;

(f) a switch forming area which includes switch circuits connected between said first data lines and data transfer lines; and

(g) a precharge circuit forming area which includes precharge circuits connected between said first data lines and said second data lines,

wherein said semiconductor integrated circuit device further includes:

(h) first lines which are formed on a second layer different from said first layer and connected in said first connecting area to said first data lines; and

(i) second lines which are formed on said second layer

and connected in said second connecting area to said second data lines,

said switch forming area being formed between said sense amplifier area and said first connecting area, with lines different from said first and second lines and formed on said second layer over said switch forming area and said precharge circuit forming area.

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